COURSE SYLLABUS
CSCI 355: DIGITAL LOGIC AND COMPUTER ORGANIZATION, FALL 2024

Class Time and Locations

Section	Schedule
F24N01	Lecture 210/240 Mon 10:00–11:30 Lecture 210/240 Wed 10:00–11:30 Lab 315/115 Tue 14:30–16:30
F24N02	Lecture 210/240 Mon 10:00–11:30 Lecture 210/240 Wed 10:00–11:30 Lab 315/115 Tue 16:30–18:30

The Lectures and Lab will be in-person face-to-face. There are no labs scheduled for the first week of classes. Labs begin on Tuesday, September 10th, 2024.

Instructor Information

Instructor:	Ajay Shrestha
Office:	Bldg 315 Room 206
Phone:	250-753-3245 Ext 2326
E-mail:	ajay.shrestha@viu.ca
Office Hours:	Mondays: 11:30 – 12:00 Wednesdays: 11:30 – 12:00

Except for holidays and weekends, I will respond to your emails within 24 hours of receiving them. Occasionally, I will send emails to the class. So, please make sure you check your email regularly.

Course Website/Learning Management System

Access at: VIU Learn
Faculty Webpage: http://csci.viu.ca/~shresthaa

Course Prerequisites

MATH 123 and min. "C" in each of CSCI 162 and CSCI 261.

Course Objective

To introduce basic principles of digital logic design, its implementation, and applications

Learning Activities

for the student:

- design, analyze and simulate digital circuits
- understand the fundamentals of digital design
- introduce microcomputer design fundamentals
- overview concepts in design verification

for the course:

- provide a sound basis for later courses in related areas
- integrate Verilog into a traditional logic design course

Overall, this course is intended for everyone who wants to understand how to design and build digital circuits.

Topics

- Binary number systems
  - Decimal to binary
  - Binary to decimal
  - Hexadecimal
  - 2's Complement Binary
- Codes
  - ASCII
  - Gray Code
- Boolean algebra
  - Proof of Boolean properties
  - Use of DeMorgan's theorems
  - Product of Sums
  - Sums of Products
  - Logic simplification (by applying Boolean algebra)
  - NAND/OR and NOR/AND equivalence
  - Karnaugh Maps
- Physical Logic Gates
  - Construct logic functions using CMOS transistors
  - Power consumption
  - Transmission gates
- Combinational logic and circuits
  - Ripple Carry Adders
  - Carry Lookahead Adders
  - Multiplexers (Shannon Expansion Theorem)
  - Decoders
  - Encoders
  - Comparators
- Sequential logic and circuits
  - RS Latches
  - Gates D Latches
  - D Flip Flops
  - JK Flip Flops
  - Registers
  - Shift Registers
  - Asynchronous Counters
  - Synchronous Counters
  - Ring Counters
  - Johnson Counters

- Synchronous Sequential Circuit Design
  - Moore/Mealy Model
  - Optimizing using Karnaugh Maps
  - Using D Flip Flops
  - Using JK Flip Flops
- Synchronous Sequential Circuit Analysis
  - State minimization
- Verilog Hardware Description Language (limited)

Recommended Lecture Texts:

Digital Design 3rd ed. (Prentice Hall) M. Morris Mano
or
Principles of Digital Design (Prentice Hall) Gajski
or
Introduction to Logic and Computer Design (McGraw/Hill) Marcovitz

Recommended Lab Texts:

Verilog for Digital Design (Wiley) Frank Vahid and Roman Lysecky

There is NO REQUIRED lecture and Lab text. A copy of Digital Design Essentials (previously used text) can be found in the lab.

Student Evaluation

Grading Scheme:

Max of 8 Lab exercises/assignments	32%
One final lab Exam on Verilog (Dec 6)	8%
Attendance and participation	5%
Midterm Exam (TBD)	20%
Final Exam (data TBD)	35%
Total	**100%**

NOTE: Students must receive a passing mark (>= 50%) on both Lab and Lecture portions separately in order to pass the course.

Evaluation of Academic Achievement

Late Policy & Other Assessment Policies
Late Work Policy
Late assignments will not be accepted.
There are no make-up tests.
All missed tests/Lab assignments will receive a zero for a grade.
However, if a student is unable to attend a lecture/lab or to complete an assessment on time for a valid reason they will be accommodated if they communicate their needs promptly.

For final grading, the following scale will be used. The instructor reserves the right to lower the numerical score required for a particular letter grade if that seems appropriate, but the same conversion will be applied to all persons in the class. Under no circumstances will the numerical score required for a particular letter grade be raised.

Grade	Percentage
A+	90-100%
A	85-89%
A-	80-84%
B+	76-79%
B	72-75%
B-	68-71%
C+	64-67%
C	60-63%
C-	55-59%
D	50-54%
F	0-49%

Institutional Grade Scale

Grade Scale: University, Career/Technical, Adult Basic Education Programs

Grade Descriptors

A+, A, A-	Outstanding performance and exceptional work. Considerable evidence of original thinking; demonstrated outstanding capacity to analyze and synthesize; evidence of extensive knowledge base.
B+, B, B-	Good performance and work has no major weaknesses. Evidence of grasp of subject matter, some evidence of critical capacity and analytical ability; reasonable understanding of relevant issues.
C+ , C, C-	Satisfactory performance and adequate work. Shows fair comprehension of the subject matter and the ability to develop solutions to simple problems.
D	Marginal performance demonstrating a minimally acceptable familiarity with subject matter, critical and analytical skills.
F	Failing work – unsatisfactory performance or failure to meet course requirements.

Regrade policy

At times, you may feel that marks were unfairly deducted during an assignment or a test. In this situation, you can submit your work for a regrade.
We will only take regrades if they are submitted within 7 days of the marks for that assignment being released.
Also, note that we reserve the right to regrade the entirety of any assignment submitted. When requesting a regrade, your old grade will be removed, and your new grade could be higher or lower.

Midterm Exam

The midterm is scheduled for Monday, either Oct 21st or 28th (will confirm in the first week) in the lecture class Bld-210/240. The midterm will consist of some short answer questions and some coding questions. Additional information will be communicated to the students in the regular classes and announced on the course *VIULearn* page (https://learn.viu.ca/d2l/loginh) closer to the actual exam date.

Lab Exam - Quiz

A lab quiz will be open for all 24 hours during all of December 6 on the course VIULearn page (https://learn.viu.ca/d2l/loginh). It will consist of some Verilog coding questions. Additional information will be communicated to the students in the regular classes and announced on the course *VIULearn* page closer to the actual quiz date.

Final Exam Scheduling

The Registrar schedules all final examinations beginning Monday, December 9th, including deferred and supplemental examinations.

Students are advised not to make travel arrangements for the exam period until the official exam schedule has been posted.

Note: All students must be properly registered in order to attend lectures and receive credit for this course.

Academic Integrity Statement

It is expected that students will know and abide by the VIU's policy on Student Academic Code of Conduct (Policy 96.01)

Standards of Academic Integrity

Include, but are not limited to:

- Independently producing work submitted under their own name
    - All graded work needs to be written independently, unless expressly instructed to collaborate
- Properly and appropriately referencing all work
- Identifying all collaborators in work
- Completing examinations without giving or receiving assistance, excepting those students requiring assistance due to a documented accessibility issue
    - The use of tutorial services, including online sites, to solve graded work is strictly prohibited
    - The use of online sites and apps for solving mathematical problems on graded work is strictly prohibited
- Respecting the integrity of examination materials and/or the examination process; and respecting the integrity of computer security systems, software copyrights and file privacy of others

Any academic misconduct will be dealt with in accordance with policies in effect at VIU (96.01) and may result in a final grade of "F", a report to the Dean and a permanent record in the student's academic file. Multiple records may result in suspension from the University.

Academic Integrity
Student Academic Code of Conduct
Policy 96.01

Lab & Lecture Pass Requirement

Students will receive a single, final grade assessing their performance in the lab and lecture components combined. Students must achieve separate passing grades in the laboratory

component and in the lecture component of the course in order to be able to earn an overall passing grade in the course.

As per Policy 95.05, if all laboratory grades are known prior to the final examination, students who have not obtained a grade of at least "D" may not be permitted to write the examination.

Laboratory Work
Policy 95.05

Attendance Requirement & Absenteeism

Students are expected to attend scheduled lectures, laboratories, field trips, seminars, examinations, practical and work experience. The University reserves the right to cancel registration in any course or program because of lack of attendance (where attendance is deemed by the Department to be important).

VIU reserves the right to cancel any student's registration in a course if the student does not attend the first scheduled session of a course and does not notify the instructor or area secretary.

Absenteeism

Students are responsible for all material presented and discussed in lecture, in addition to assigned readings and homework problem. It is entirely the students' responsibility to recover any information or announcements presented in lectures from which they were absent by speaking to their fellow students.

Students who are absent should contact their instructors as soon as possible and report to their instructors again on return to classes. Extended absence from courses or program should be discussed with each instructor or program coordinator involved. Students are responsible for contacting their instructors, either directly or through the assistance of staff in the office of the appropriate Dean, as soon as an extended absence becomes apparent.

Specific regulations exist for absences due to illness, death in the family, religious observances, and VIU official sporting teams. In cases of religious observance and sporting events, discussion on the impact of your absence with your instructor needs to occur at least two weeks in advance of the absence.
Attendance and Absences | Policy 96.05

Student Code of Conduct/Conduct in Class

It is expected that students will always treat one another and the instructor with respect and dignity. Alcohol and drug use is prohibited during any course period, and in the hours prior to any laboratory/field/practicum period where impaired functioning is a safety hazard.

Student Code of Conduct (Non-Academic) | Policy 32.05

EDI Statement

VIU values human diversity in all its dimensions and is committed to achieving and ensuring learning and working environments that are equitable, diverse and inclusive.

Academic Plan | EDI Action

Other Supports (Advising, Counselling, Writing Center, Math Learning Centre, Accessibility Services)

VIU hosts numerous Learning Supports for student success and you are encouraged to take advantage of them. Links to each can be found on the Resources for Students page. Students are strongly encouraged to review the information provided by Accessibility Services, Advising, Counselling, Math Learning Centre, the Office of Indigenous Education and Engagement, and the Writing Center.

Changes to the Syllabus

There may be revisions to the outline that are required once the semester begins.
If this happens, the syllabus will be updated, and students will be notified of the revision promptly.
If a revision is made to the syllabus, the intent is that the modification will be advantageous to the student.

Land Acknowledgement

We acknowledge and thank the Snuneymuxw, Quw'utsun and Tla'amin, on whose traditional lands we teach, learn, research, live and share knowledge. We pay our respect to the First Nations ancestors of this place and reaffirm our relationship with one another.